UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,483	03/01/2002	Kazuo Kobayashi	81754.0072	5100

26021 7590 02/23/2005

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
PIZIALI, JEFFREY J	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,483	KOBAYASHI, KAZUO	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 November 2004 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The listing of references in the specification (see pages 3-4 for instance) is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Cairns et al. (US 6,437,767).

Regarding claim 1, Cairns discloses a semiconductor integrated circuit that supplies a plurality of display signals [Fig. 9; AVIDEO] to a corresponding plurality of signal electrodes of an image display apparatus [Fig. 9; 50] that displays a two-dimensional image, and successively supplies scanning signals [Fig. 9; L1-LN, R1-RN] to a first group of scanning electrodes [Fig. 9; 51] and a second group of scanning electrodes [Fig. 9; 52] of the image display apparatus, the semiconductor integrated circuit comprising: a storage device [Fig. 9; 56] that receives and stores image data; a display signal generation device [Fig. 9; 56A] that generates the plurality of display signals to be supplied to the plurality of signal electrodes based on data stored in the storage device; a first scanning signal generation device [Fig. 9; 53] that successively generates scanning signals [Fig. 9; L1-LN] to be supplied to the first group of scanning electrodes based on a clock signal [Fig. 13a; HSYNC] that defines a scanning timing of the image display apparatus, wherein each scanning signal enables all of the scanning electrodes on a scanning line; a second scanning signal generation device [Fig. 9; 54] that successively generates scanning signals [Fig. 9; R1-RN] to be supplied to the second group of scanning electrodes based on the clock signal,

wherein each scanning signal enables all of the scanning electrodes on a scanning line; and a timing control device [Fig. 13a; HSYNC, 75, 76] that generates the clock signal, and generates a first timing control signal [Fig. 13a; SSYNC1] for controlling the first scanning signal generation device and a second timing control signal [Fig. 13a; SSYNC1] for controlling the second scanning signal generation device such that the first scanning signal generation device and the second scanning signal generation device generate the scanning signals in a specified order, wherein the first scanning signal generation device outputs a first scanning signal [Figs. 9 & 10; L3] successively to the first group of scanning electrodes based on the first control signal, and wherein the second scanning signal generation device outputs a second scanning signal [Figs. 9 & 10; R2] successively to the second group of scanning electrodes based on the second control signal (see Figs. 10 & 14; Column 8, Line 26 - Column 9, Line 9 and Column 10, Line 24 - Column 11, Line 21).

Regarding claim 2, Cairns discloses the first scanning signal generation device generates the scanning signals to be supplied to the first group of scanning electrodes based on a logical product [Fig. 13a; 76] of the clock signal and the first timing control signal, and the second scanning signal generation device generates the scanning signals to be supplied to the second group of scanning electrodes based on a logical product of the clock signal and the second timing control signal (see Column 10, Line 24 - Column 11, Line 21).

Regarding claim 3, this claim is rejected by the reasoning applied in the above rejection of claim 1; furthermore Cairns discloses a first scanning signal generation device [Fig. 9; 53] that

successively generates scanning signals [Fig. 9; L1-LN] to be supplied to the first group of scanning electrodes [Fig. 9; 51] based on the clock signal [Fig. 13a; HSYNC] and a first set potential [Fig. 13a; SSYNC1]; wherein each scanning signal enables all of the scanning electrodes on a scanning line; a second scanning signal generation device [Fig. 9; 54] that successively generates scanning signals [Fig. 9; R1-RN] to be supplied to the second group of scanning electrodes [Fig. 9; 52] based on the clock signal and a second set potential [Figs. 13a & 14; SSYNC1], wherein each scanning signal enables all of the scanning electrodes on a scanning line; wherein the first scanning signal generation device includes a first shift register [Fig. 15; 80], a first shift register control circuit [Fig. 13a; HSYNC, 75, 76] that controls the operation of the first shift register, and a first scanning side drive circuit [Fig. 15; 81] that outputs scanning signals to the first group of scanning electrodes of the liquid crystal panel based on output signals of the first shift register, and wherein the second scanning signal generation device includes a second shift register [Fig. 14; 80], a second shift register control circuit [Fig. 13a; HSYNC, 75, 76] that controls the operation of the second shift register, and a second scanning side drive circuit [Fig. 14; 81] that outputs scanning signals to the second group of scanning electrodes of the liquid crystal panel based on output signals of the second shift register (see Column 10, Line 24 - Column 11, Line 351).

Regarding claim 4, Cairns discloses one of the first and second set potentials is a power supply potential, and the other one is a ground potential (see Fig. 13b; Column 10, Line 24 - Column 11, Line 21).

Regarding claim 5, this claim is rejected by the reasoning applied in the above rejection of claim 1; furthermore Cairns discloses a first scanning signal generation device [Fig. 9; 53] that successively generates scanning signals [Fig. 9; L1-LN] to be supplied to the first group of scanning electrodes [Fig. 9; 51] based on a first timing control signal [Fig. 13a; SSYNC1]; wherein each scanning signal enables all of the scanning electrodes on a scanning line; a second scanning signal generation device [Fig. 9; 54] that successively generates scanning signals [Fig. 9; R1-RN] to be supplied to the second group of scanning electrodes [Fig. 9; 52] based on a second timing control signal [Fig. 13a; SSYNC1]; wherein each scanning signal enables all of the scanning electrodes on a scanning line; wherein the timing control circuit controls output timings of the first and second scanning signals at the first scanning signal generation device and the second scanning signal generation device, and wherein the timing control device outputs first pulses [Figs. 13b & 14; SSYNC2] to a first line that are clock signals that determine timings for line scanning at the first scanning signal generation device, and outputs second pulses [Figs. 13b & 14; SSYNC2] to a second line that are clock signals that determine timings for line scanning at the second scanning signal generation device (see Figs. 13b & 14; Column 10, Line 24 - Column 11, Line 21).

Regarding claim 6, Cairns discloses the first scanning signal generation device and the second scanning signal generation device alternately generate the scanning signals (see Fig. 10; Column 8, Line 26 - Column 9, Line 9).

Regarding claim 7, Cairns discloses a panel [Fig. 9; 50] having the first group [Fig. 9; 51] and second group [Fig. 9; 52] of scanning electrodes disposed such that scanning signals to be supplied to the first group of scanning electrodes are input in one direction of the first group of scanning electrodes (see Fig. 9; Column 8, Line 26 - Column 9, Line 9), and scanning signals to be supplied to the second group of scanning electrodes are input in the other direction of the second group of scanning electrodes; and a substrate that mounts the panel and the semiconductor integrated circuit thereon (see Column 11, Lines 22-35).

Regarding claim 8, Cairns discloses the first scanning signal generation device comprises: a first shift register [Fig. 15; 80]; and a first driver circuit [Fig. 15; 81] coupled to the first shift register, said first shift register receiving the clock signal and/or the first timing control signal for successively generating a drive signal [Fig. 14; L1, L2] to one of a plurality of input terminals of said first driver circuit, said first driver circuit then successively outputting a scanning signal to predetermined scanning electrodes [Fig. 15; 51] of the first group of scanning electrodes (see Column 10, Line 58 - Column 11, Line 35).

Regarding claim 9, Cairns discloses the second scanning signal generation device comprises: a second shift register [Fig. 14; 80]; and a second driver circuit [Fig. 14; 81] coupled to the second shift register, said second shift register receiving the clock signal and/or the second timing control signal for successively generating a drive signal [Fig. 14; R1, R2] to one of a plurality of input terminals of said second driver circuit, said second driver circuit then

successively outputting a scanning signal to predetermined scanning electrodes of the second group of scanning electrodes (see Column 10, Line 58 - Column 11, Line 35).

Regarding claim 10, this claim is rejected by the reasoning applied in the above rejection of claim 2; furthermore Cairns discloses the first scanning signal generation device comprises a first control circuit [Fig. 13a; HSYNC, 75, 76] for generating a first control signal [Fig. 13a; SSYNC1] based on the first set potential, and the second scanning signal generation device comprises a second control circuit [Fig. 13a; HSYNC, 75, 76] for generating a second control signal [Fig. 13a; SSYNC1] based on the second set potential (see Fig. 14; Column 10, Line 24 - Column 11, Line 21).

Regarding claim 11, this claim is rejected by the reasoning applied in the above rejection of claims 1, 8, and 9.

Regarding claim 12, Cairns discloses the step of generating first and second control signals comprises: generating a clock signal [Fig. 13a; HSYNC]; and alternately generating the first and second control signals [Fig. 13a; SSYNC1] based on the clock signal (see Fig. 13b; Column 10, Line 24 - Column 11, Line 21).

Regarding claim 13, this claim is rejected by the reasoning applied in the above rejection of claims 2 and 12.

Regarding claim 14, this claim is rejected by the reasoning applied in the above rejection of claims 2 and 3.

Regarding claim 15, this claim is rejected by the reasoning applied in the above rejection of claim 4.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 3 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 3 recites the limitation "the liquid crystal panel" in lines 22 and 27-28. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 5 recites the limitation "the timing control circuit" in line 20. There is insufficient antecedent basis for this limitation in the claim.

Response to Arguments

10. Applicant's arguments filed 23 November 2004 have been fully considered but they are not persuasive. The applicant contends the cited prior art of Cairns et al. (US 6,437,767) neglects to teach "wherein each scanning signal enables all of the scanning signals on a scanning line" (see page 12 of the amendment filed 23 November 2004). However, the examiner respectfully disagrees. On the contrary, Cairns states, "Each row of pixels within the AMLCD 50 of N rows and M columns has two scan lines 51 and 52, the scan line 51 connecting the gates of the TFT's of the left hand group of pixels to a left hand scan line driver circuit 53 and the scan line 52 connecting the gates of the TFT's of the right hand group of pixels to a right hand scan line driver circuit 54. The scan lines 51 and 52 do not overlap..." (see Fig. 9; Column 8, Lines 28-36). As such, Cairns most certainly does teach each scanning signal enabling all of the scanning signals on a scanning line. And by such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J.P.
22 February 2005

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600